**ELEC 204 Digital Design Lab Report**

Lab 5

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1. **Introduction and objectives**

The main objective in this lab is to develop a state machine with timers and external asynchronous inputs. Then, we aim to use the state machine design for implementing its logic circuit design.

A state machine (or a finite-state machine) is a device or an algorithm, which can be in one of a set number of stable conditions depending on its previous condition and on the present values of its inputs.

In this experiment, we have shown:

* ekran görüntüsü içeren bir resim

  Açıklama otomatik olarak oluşturuldudesign a state diagram of a washing machine,
* implement its corresponding state diagram on FPGA using a modular design,
* experimentally demonstrate the operation of the state machine.

My code tries to do simulate a washing machine. In typical washing machine there is a couple of states, which are washing, rinse, spin and etc. Our main purpose in this lab developing State machine with asynchronous inputs.

1. **Methods**

Three inputs:

Start -> (1 bit) to start state diagram

Reset-> (1 bit) goes to the starting state immediately

Clk -> typical clock comes from board with (1 bit)

4 outputs:

ZERO -> (1 bit) shows change state

DEC -> (1 bit) shows state machine working not finish yet

States -> (2 bit) shows current state

Phase -> (4 bit) shows stage of machine to the user.

metin, ekran görüntüsü içeren bir resim

Açıklama otomatik olarak oluşturuldu

**Figure.** Main module

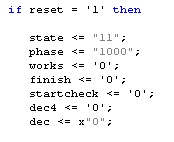
**Figure.** ucf file for LAB5

ekran görüntüsü içeren bir resim

Açıklama otomatik olarak oluşturuldu

in this lab my objective is to develop a state machine with timers and external asynchronous inputs. To do this I created 4 different states: Wash, Spin, Rinse and Idle (00,01,10,11). In this logic circuit I used inputs and counters to check switch to the next state or not.

Whenever we start our machine, we are in the initial state which is IDLE(11). I controlled states with 5 different conditions (which has 4 different states with idle state has 2 different coditions.). If we do not push start button we stay in the idle state. But if start button is pressed, machine will start to the state circuit which contolled by counter and clock. In this lab we used 4 sec for washing; 3 for spin; 2 for rinse state. After that we come back to the initial state by restoring counters and states.

Differently from this process, we can reset our process. So by this way we do not need to wait until end of the process. This button allows you to finish the process instantly. Everything comes to the initial state with 1 different thing: finish led will not light.

**Figure.** State module

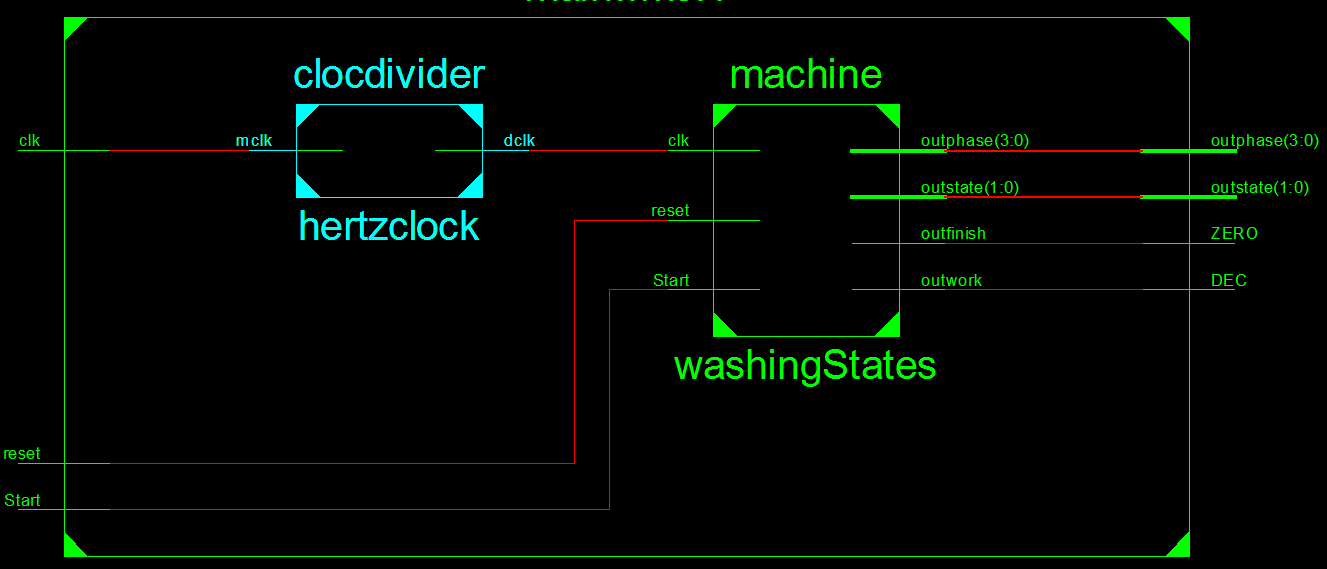
**Figure.** Reset part inside state module

ekran görüntüsü içeren bir resim

Açıklama otomatik olarak oluşturuldu

Clock divider has same idea with previous labs. In this lab I need seconds, so I used clock divider from 100MHz to 1 Hz.

**Figure.** Clock divider



**Figure.** RTL Schematics for washing machine

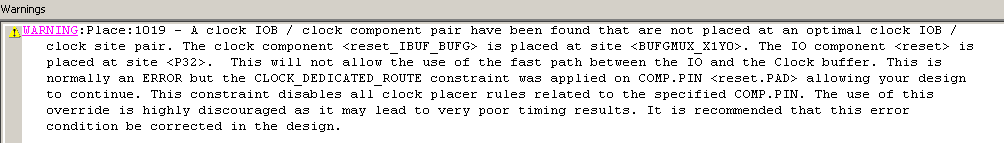
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Start | S1 | S0 | Next S1 | Next S0 | Z0 |
| 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 |

**Figure.** Truth Table for state diagram

1. **Problems encountered, errors and warnings resolved**

In this Lab I didn’t get main error, However I dropped into the combinational loop in my code. I didn’t get the reason for this problem. So, I couldn’t use ZERO input properly. That’s why I changed functionality of ZERO a little.

Also I have same warning with previous LAB which can be ignored as I understood.



**Figure.** Warning about ucf ports

1. **Conclusion**

In this experiment, we have done designing a state diagram of a washing machine. Then implemented its corresponding state diagram on FPGA board using a modular design. By this way we could experimentally demonstrate the operation of the state machine. This Lab actually useful for me, because we used state diagrams in our project, however we didn’t know how to implement and how to use properly. This lab shows where is the problem in our project. State machines are used in many fields today. In this experiment we tried to show one of the simplest of state machines.

References

1. Marro, Ciletti (2018). Digital Design. New York, NY; Pearson
2. LAB-5, ELEC-204 Digital Design Course Notes

elektronik eşyalar, devre içeren bir resim

Açıklama otomatik olarak oluşturulduelektronik eşyalar, devre içeren bir resim

Açıklama otomatik olarak oluşturuldu

**Figure.** IDLE state(initial or initated with Reset) **Figure.** Wash State

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Açıklama otomatik olarak oluşturuldu

**Figure.** Spin State **Figure.** Rinse State

elektronik eşyalar, devre içeren bir resim

Açıklama otomatik olarak oluşturuldu

**Figure.** IDLE State(state machine end)